

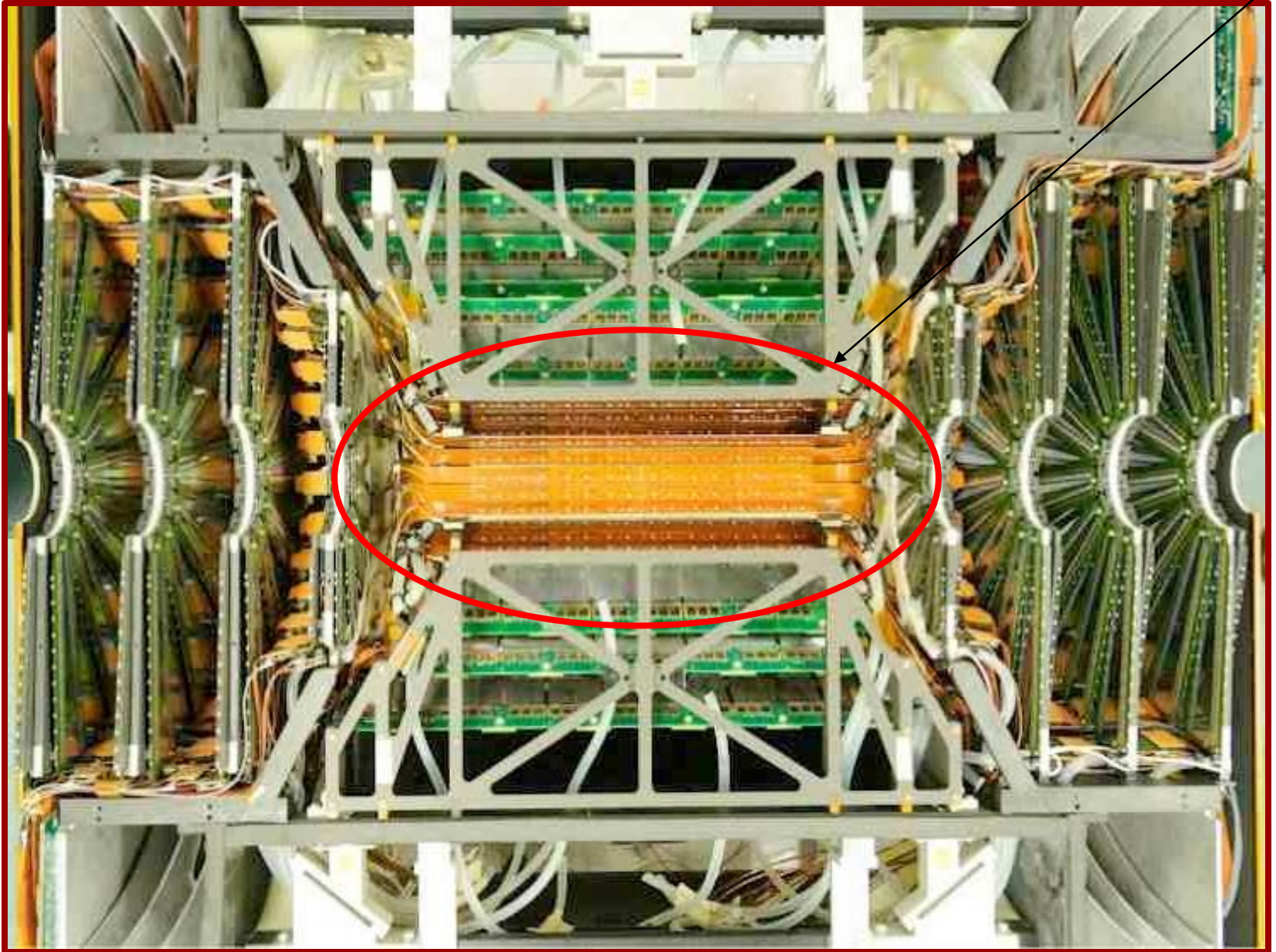
Integration of the Silicon Pixels into sPHENIX

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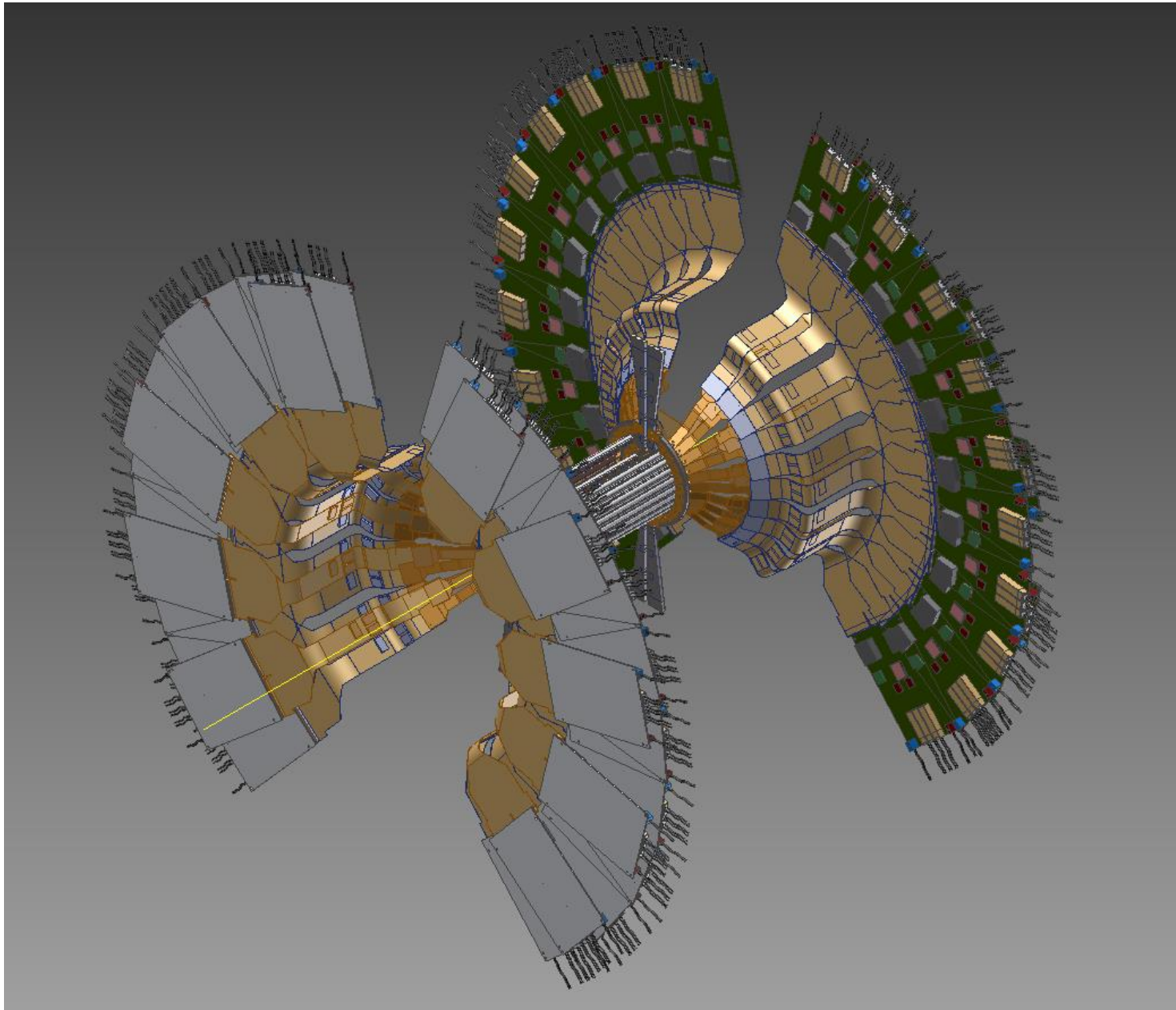
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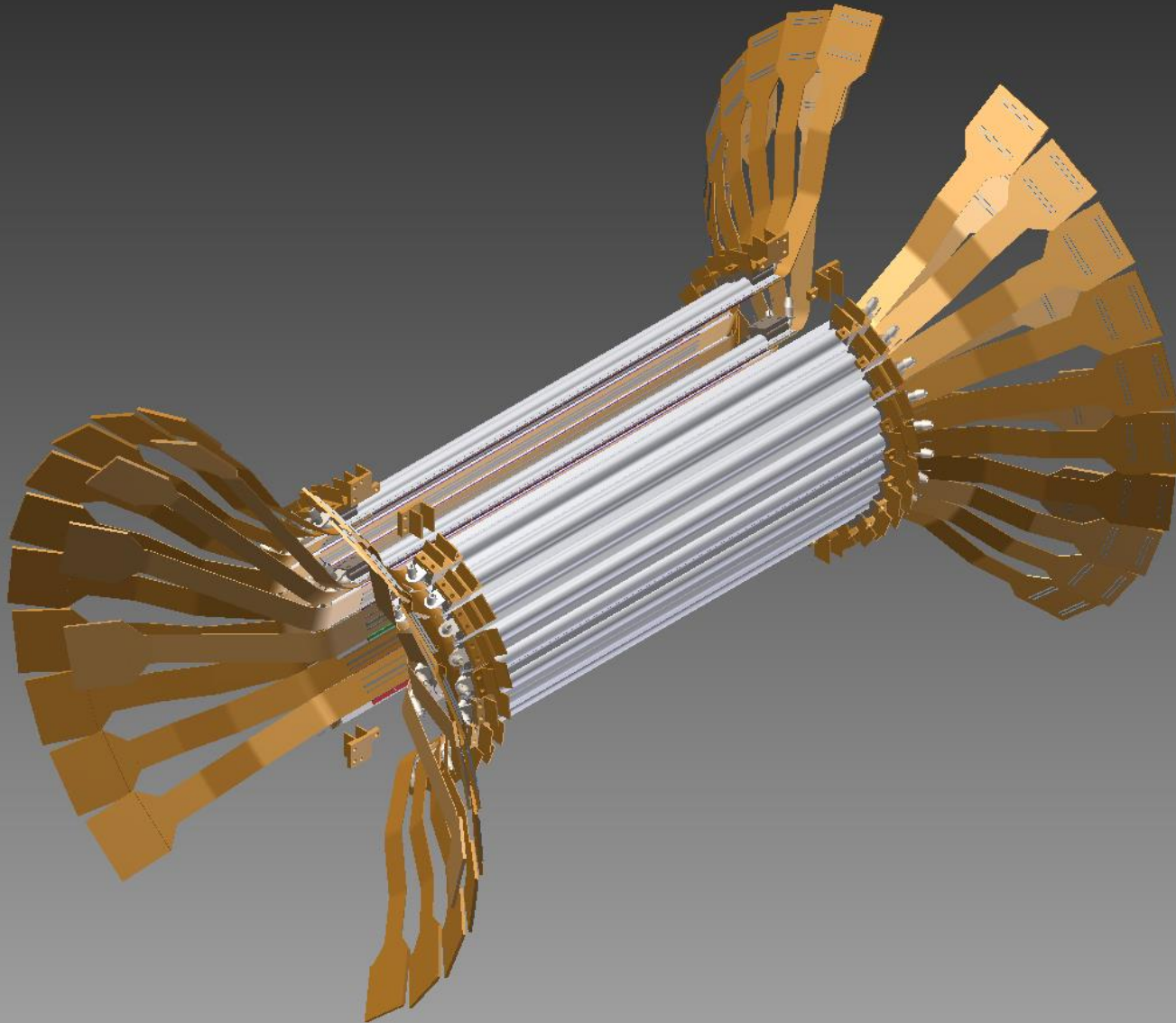
How to integrate Silicon Pixels into sPHENIX?



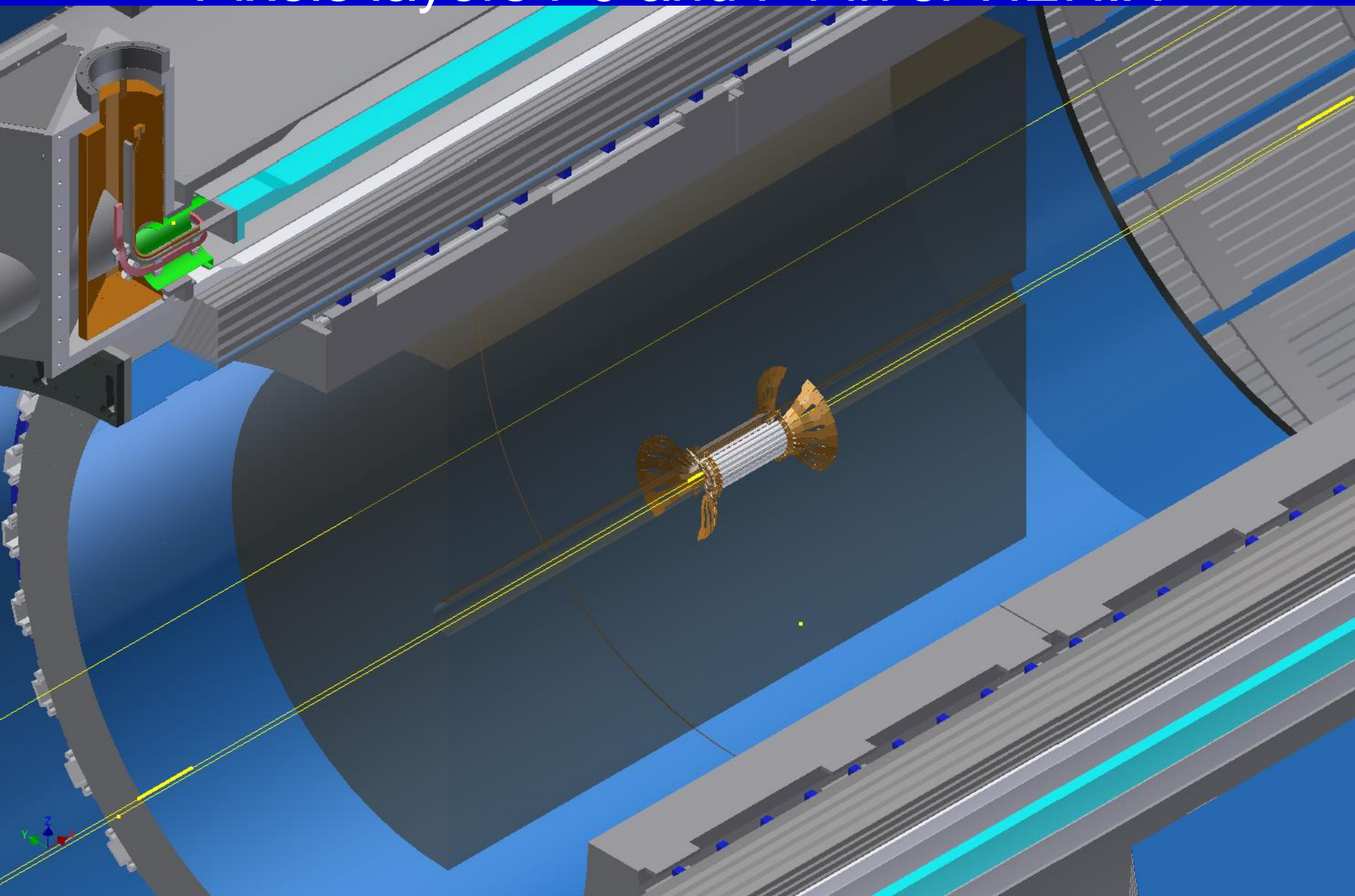
VTX Envelope: Pixels with Full Readout Chain



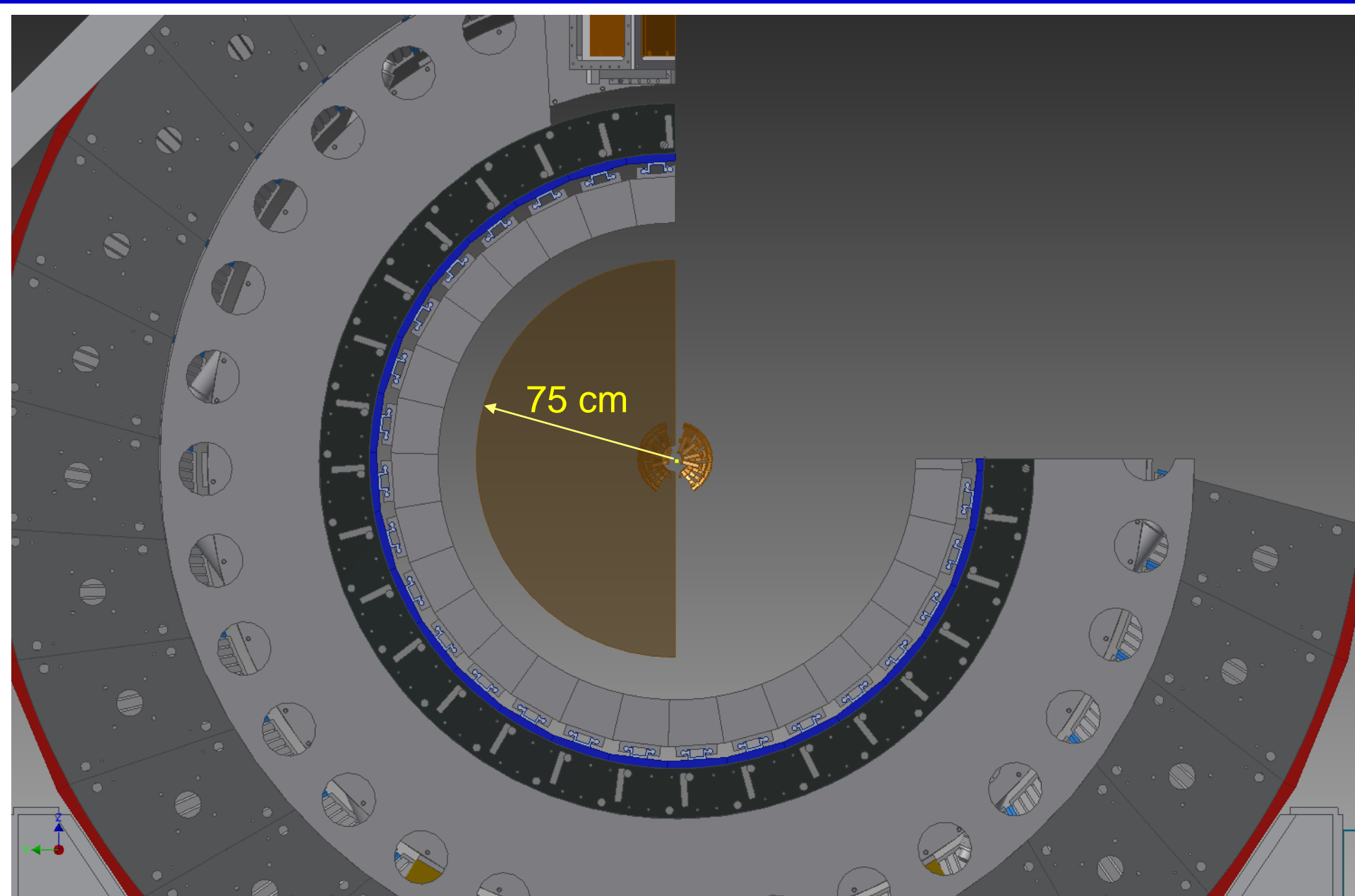
Pixels Only: P0 and P1



Pixels layers P0 and P1 in sPHENIX



Tracking Envelop in sPHENIX: 75 cm



To do List

- How many ladders are needed for P0 and P1 to have full coverage in sPHENIX?
Knowing: r_0 (P0) = 2.48 cm and r_1 (P1) = 3.63 cm.

